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NOTE 1: THIS PARTS LIST IS A SAMPLE ONLY. FOR THE PARTS LIST OF A PARTICULAR VARIATION SEE B-DD-M7891-~~7~~.

MP00672

EN-01124-16-N675-(327)

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DRAWING DIRECTORY

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NOTE: FOR FIELD MAINTENANCE PRINT SET
SEE B-TC-MS11-L-1

UNIT VARIATIONS

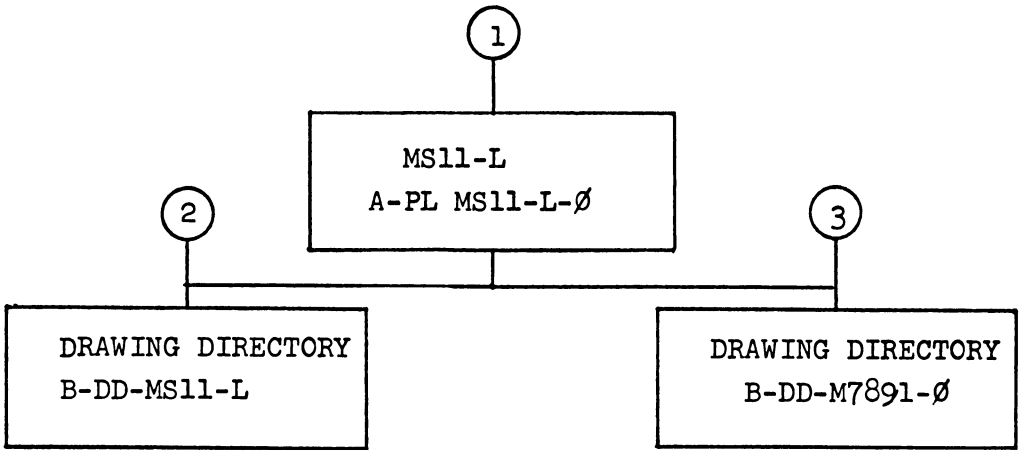
[illegible]

REVISIONS	REV.	
	CHANGE NO.	
	CHK	

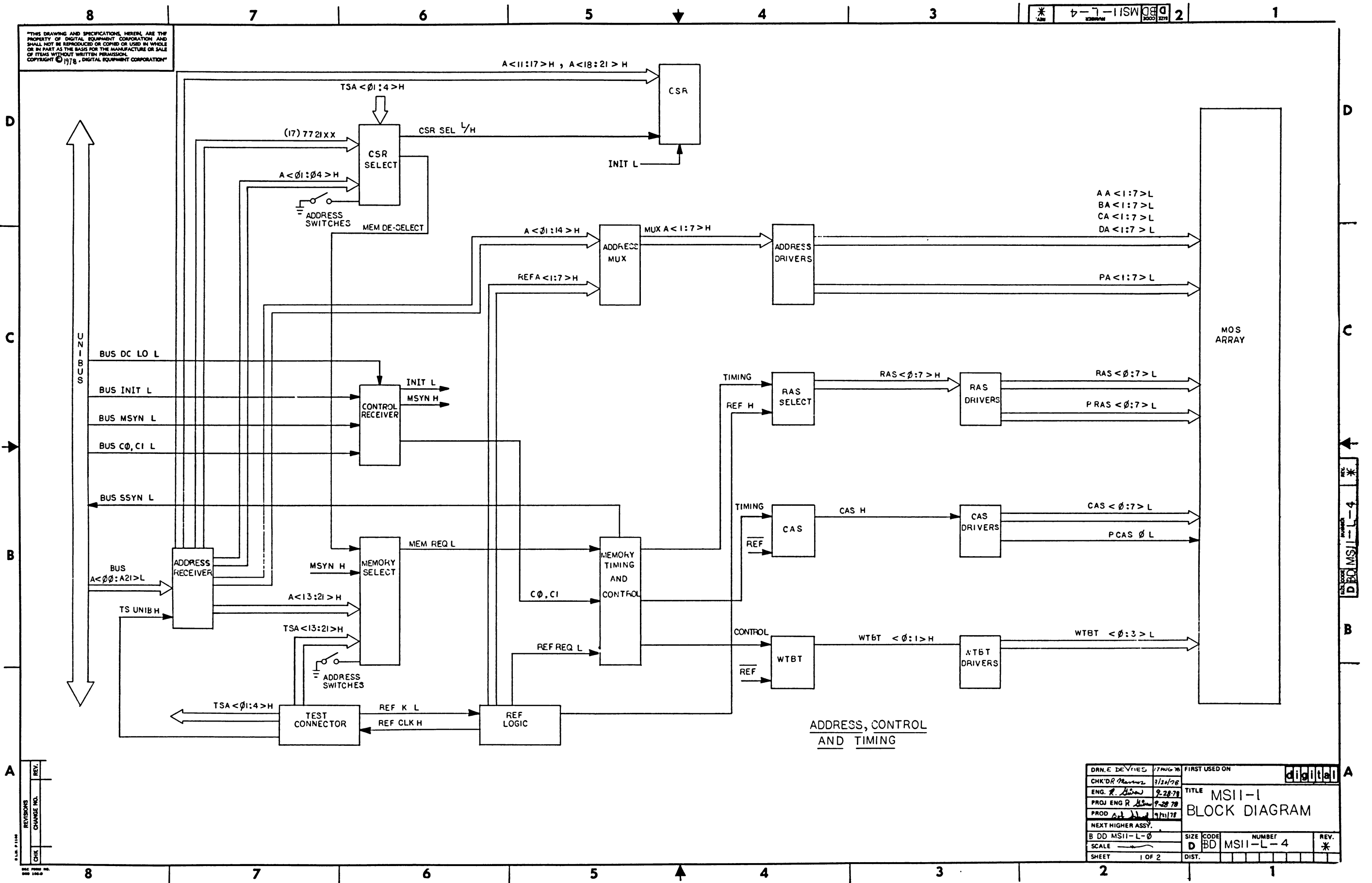
USED ON OPTION/MODEL	DRN.	DATE	TITLE										
PDP 11/34	E.DEVRIES		DRAWING DIRECTORY										
	CHK'D.	DATE	MS11 (128K X 18)										
	R. Mamon	9/26/78	MOS MEMORY SYSTEM										
	PROJ. ENG.	DATE											
	R. Given	9-28-78	SIZE	CODE	NUMBER						REV		
	PROD.	DATE	B	DD	MS11-L						*		
SHEET 1 OF 3	Bob Johnson	9/21/78	DIST.										

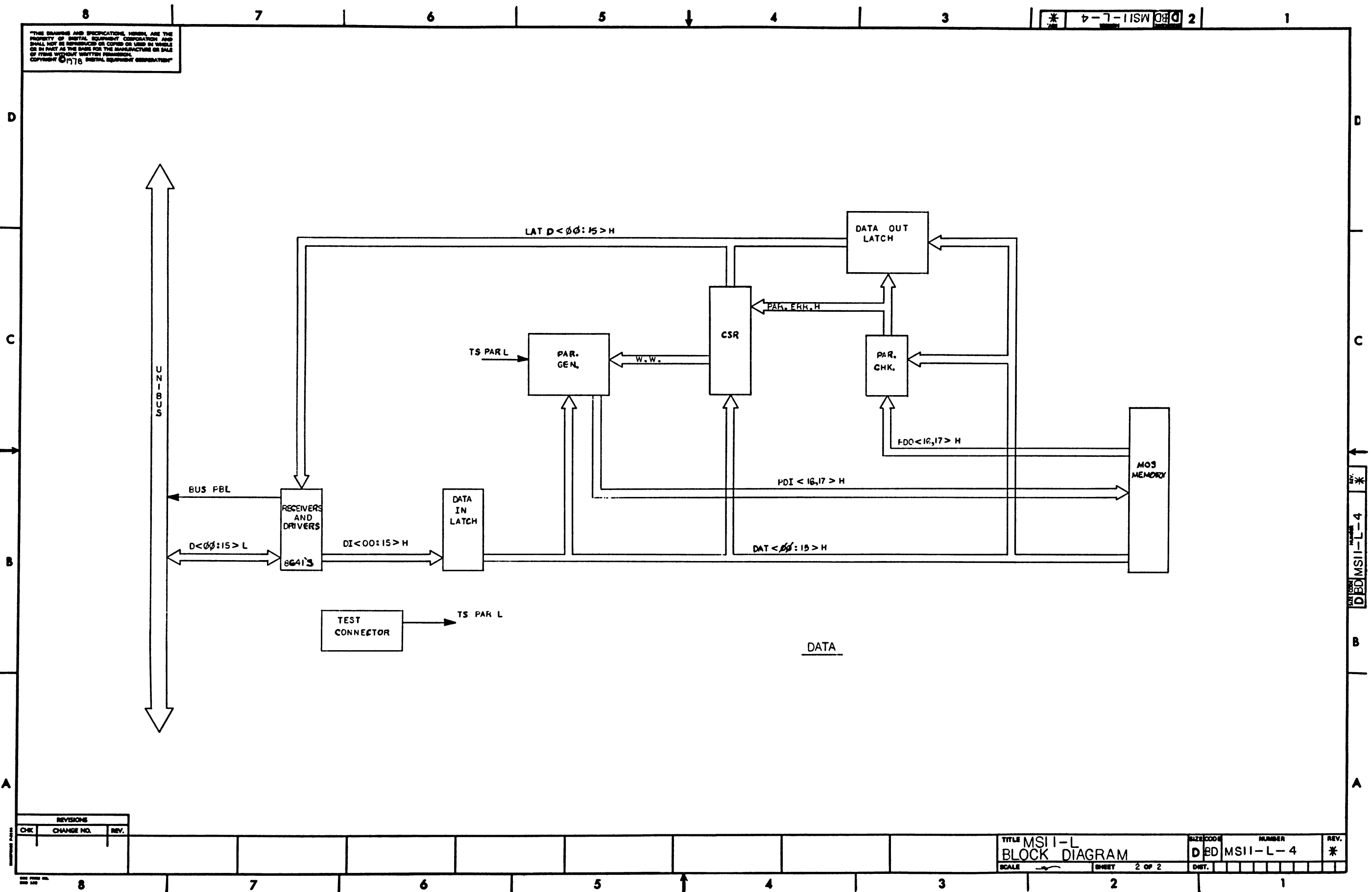
digital

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1978
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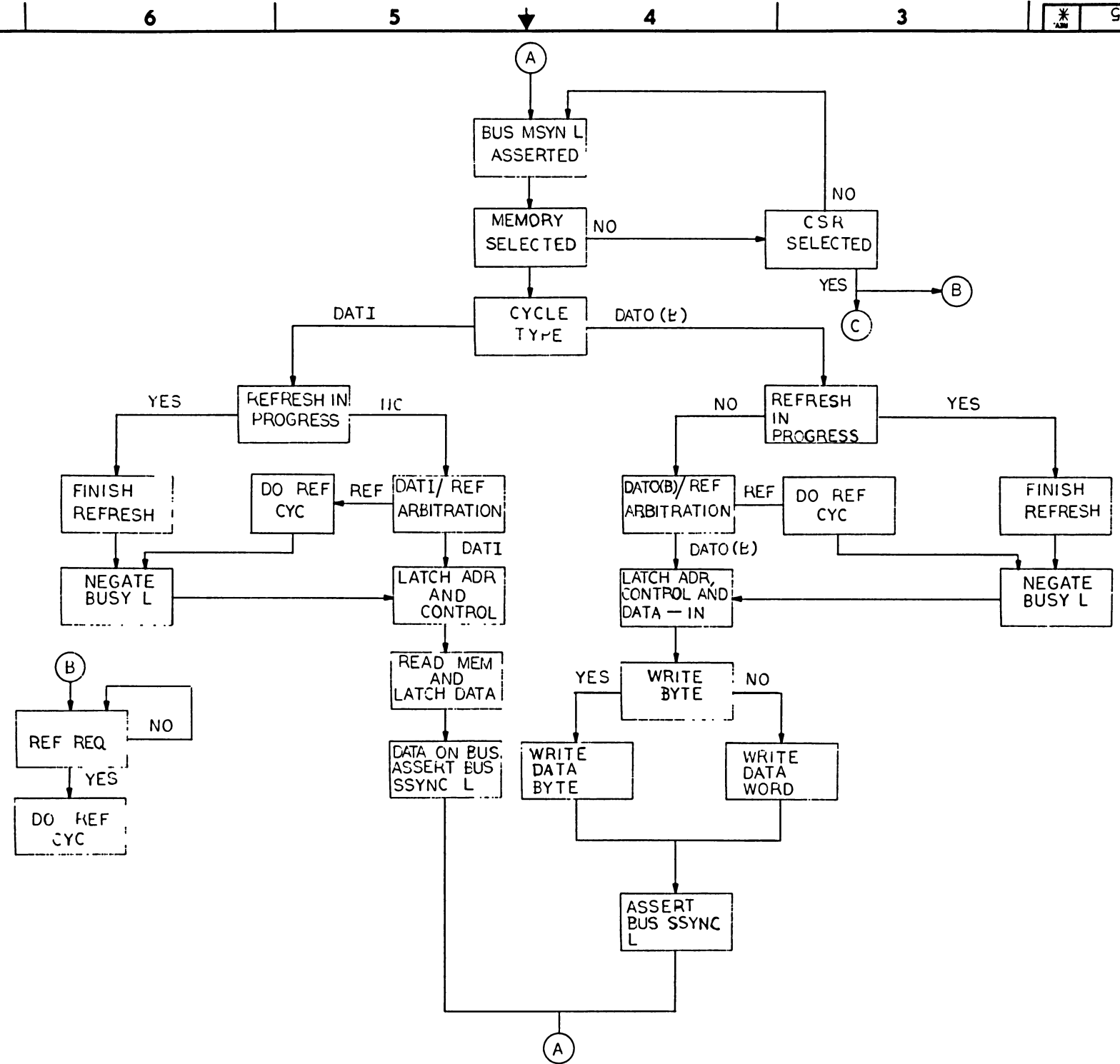
TITLE	DRAWING DIRECTORY MS11 (128K X 18) MOS MEMORY SYSTEM	SHEET 2 OF 3	SIZE B DD	CODE MS11-L	NUMBER MS11-L	REV *
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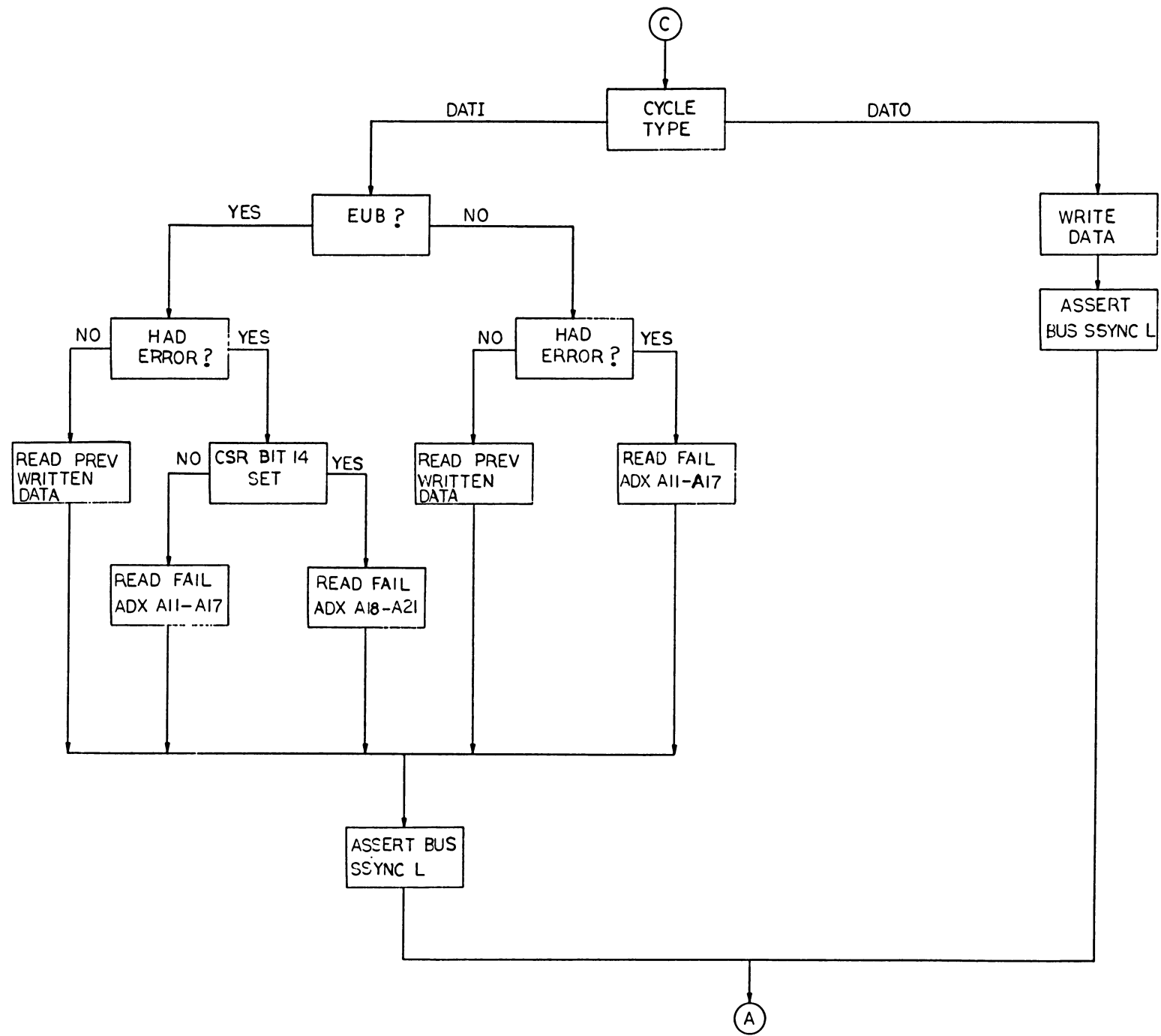
8 7 6 5 4 3 2 1

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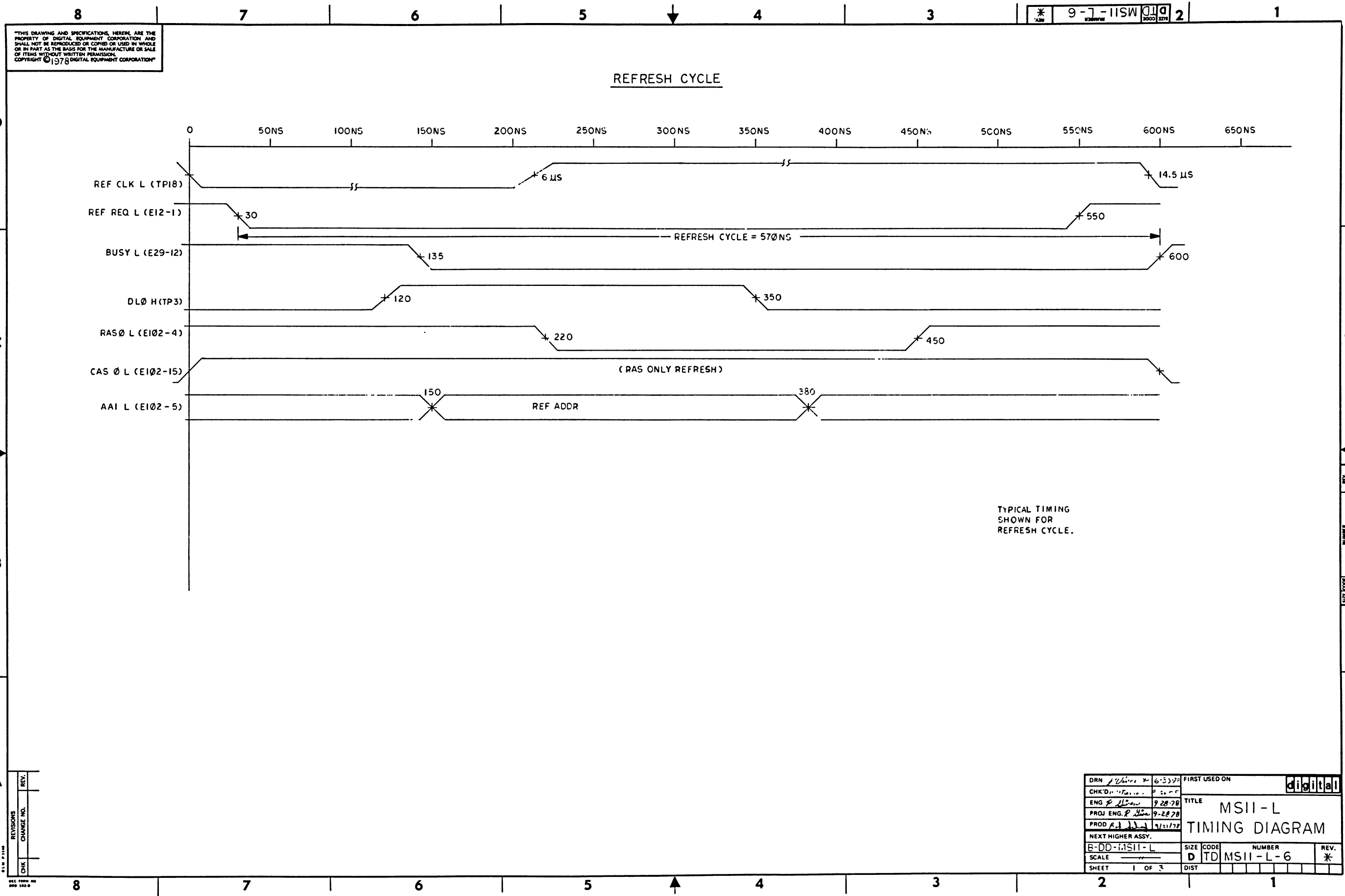
DRN 1.1.1.1.1.1.1	9-7-78	FIRST USED ON	digital
CHK'D 3 Memo 2	9/26/78	TITLE	MS11-L (DATI/DATO)
ENG. R. Brown	9-28-78	NUMBER	MS11-L-5
PROJ. ENG. P. H. H.	9-28-78	REV.	*
PROD. A. J. J.	9/28/78	SIZE	D
NEXT HIGHER ASSY.		CODE	FD
B-DD-MS11-L		DIST.	
SCALE			
SHEET 1 OF 2			

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE MSII-L (DATI/DATO)		SIZE CODE D	FD	NUMBER MSII-1 - 5	REV. *
FLOW DIAGRAM		SHEET 2 OF 2		DIST.	



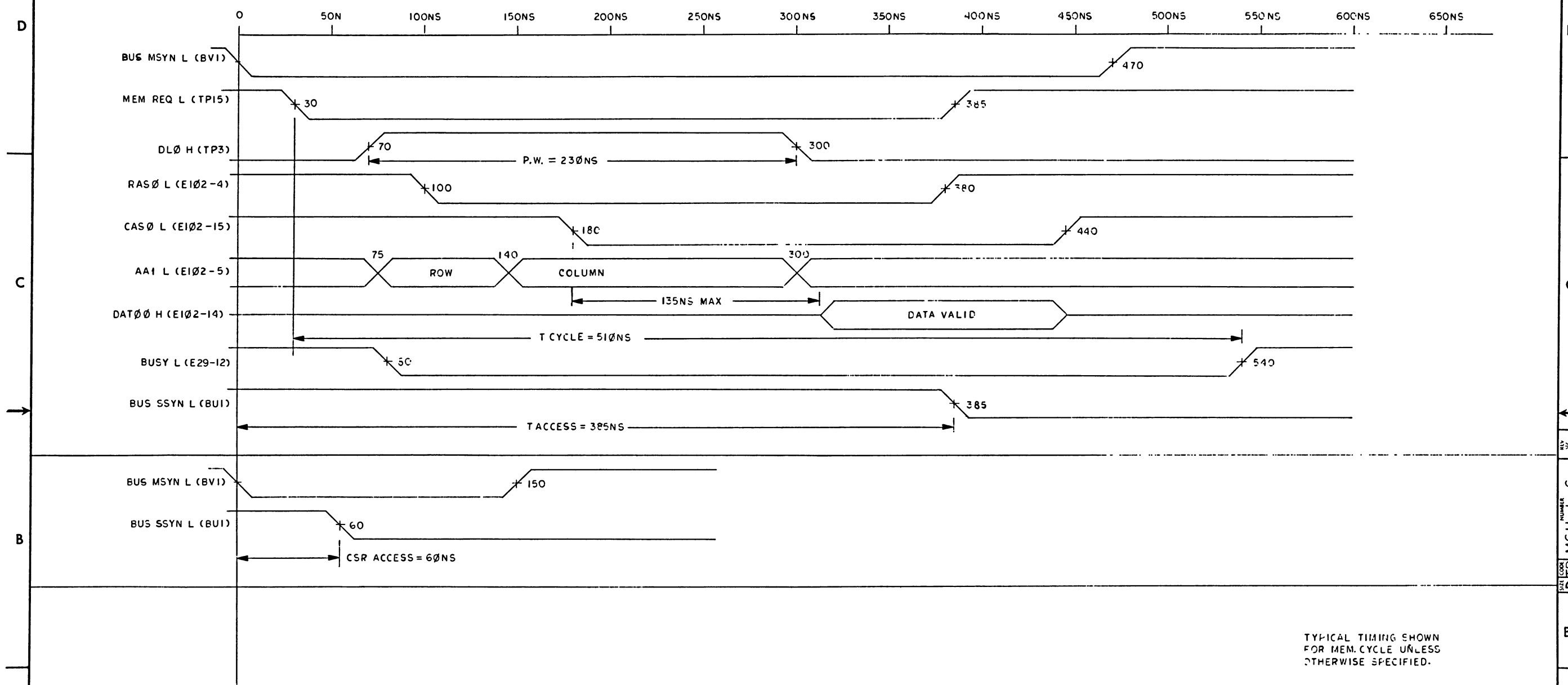
REV.	
CHG	
REV.	
CHG	
REV.	
CHG	

DRN	9-7-11SW	6-3372	FIRST USED ON	digital
CHK'D	9-28-78	9-28-78	TITLE	MS11-L
ENG	9-28-78	9-28-78	TIMING DIAGRAM	
PROJ ENG	9-28-78	9-28-78		
PROD	9-28-78	9-28-78		
NEXT HIGHER ASSY.				
B-00-MS11-L				
SCALE				
SHEET	1 OF 3			
SIZE	D	CODE	TD	NUMBER
				MS11-L-6
				REV.
				*

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REV	9-7-11SW	CODE	DATE	2
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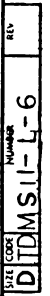
DATI CYCLE



REVISIONS		
CHK	CHANGE NO	REV

TITLE MSII-L TIMING DIAGRAM		SIZE D	CODE TD	NUMBER MSII-L-6					REV *
SCALE	SHEET 2 OF 3	DIST.							

TYPICAL TIMING SHOWN
FOR MEM. CYCLE UNLESS
OTHERWISE SPECIFIED.



MATERIALS PAGE 7114	REVISIONS													TITLE		SIZE CODE		NUMBER		REV.
	CHK	CHANGE NO.	REV											MSII-L TIMING DIAGRAM		D TD		MSII-L-6		*
														SCALE		SHEET 3 OF 3		DIST.		
DEC FORM NO DDO 135			8		7		6		5		4		3		2		1			

BLANK

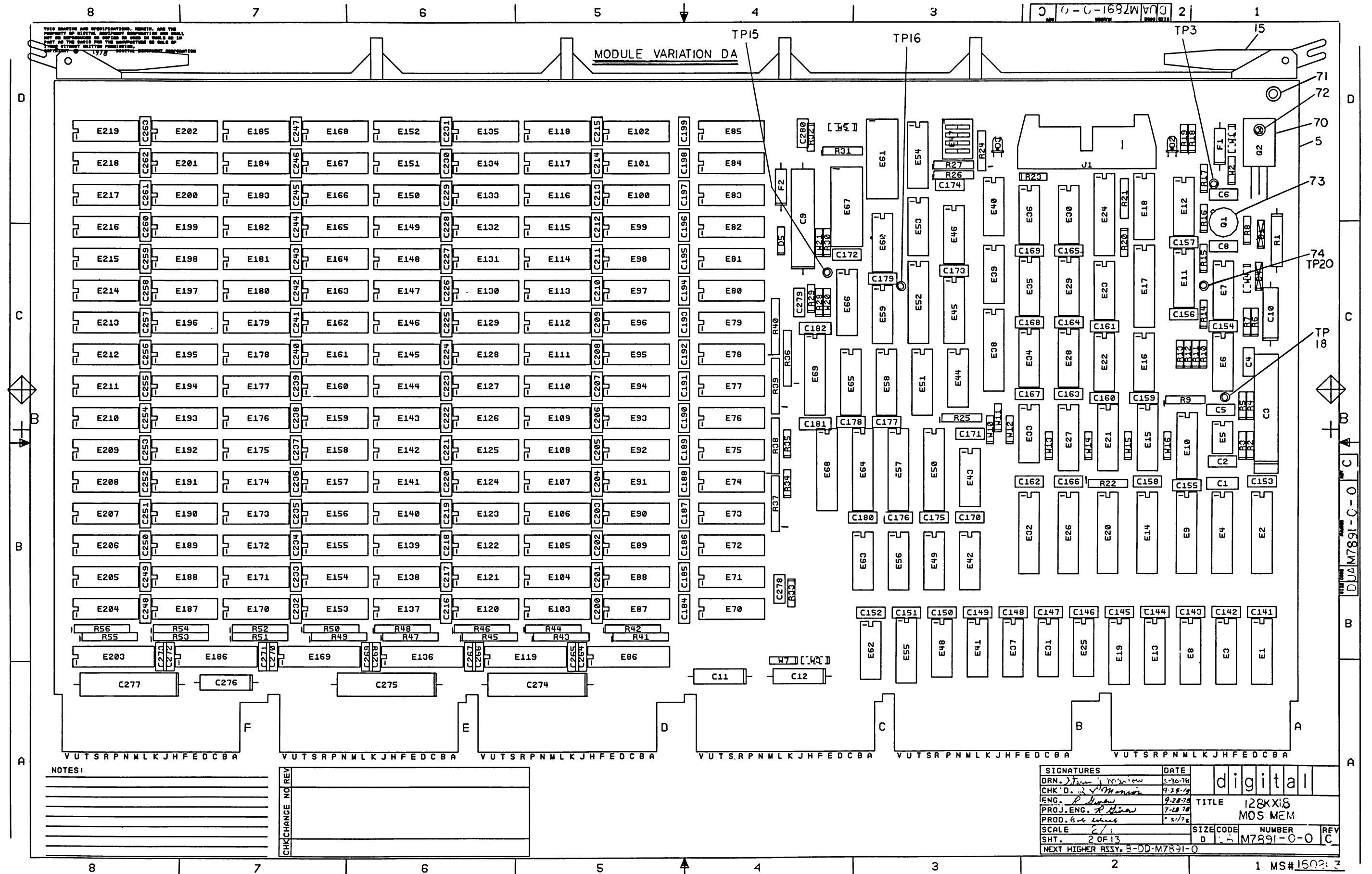
LINE	ITEM	DOCUMENT NO.	PART NO.	DESCRIPTION	QTY	REFERENCE DESIGNATORS
29	29		1303110-00	19.6 1/4W 1% RN55D-F 100PPM (13-00	1	R10
30	30		1303156-00	34.8 K 1/4W 1% RN55D-F 100PPM (13-00	1	R5
31	31		1305123-00	215 1/4W 1% RN55D-F 100PPM (13-00	1	R20
32	32		1305322-00	7.5 K 1/4W 1% RN55D-F 100PPM (13-00	1	R4
33	33		1312466-00	10 1W 1% WW (13-00	1	R1
34	34		1315678-00	R NETWORK 3-18 OHM RESISTORS 5% SIP	16	R41-R56
35	35		1315339-00	R NETWORK 4-5K RESISTORS 5% SIP	7	R9,R22,R24-R27,R31
36	36		1613120-00	DELAY= 200NS,10TAPS	1	E18
37	37		1910532-00	74S00 NAND GATE=QUAD 2IN	3	E16,E46,E53
38	38		1910533-00	74S03 NAND GATE=QUAD 2IN,OPN COLLECT	1	E7
39	39		1910536-00	74S10 NAND GATE=TRIPLE 3IN	2	E28,E39
40	40		1910537-00	74S11 AND GATE=TRIPLE 3INPUT	2	E29,E44
41	41		1910539-00	74S20 NAND GATE=DUAL 4INPUT	1	E59
42	42		1910544-00	74S74 FF-D DUAL,EDGE TRIGGER	2	E33,E34
43	43		1910544-01	74S74-60GG-D DUAL,EDGE TRIGGER,SYNCHR	1	E6
44	44		1910549-00	74S158 MUX 1 OF 2 (QUAD)	2	E58,E65
45	45		1911469-00	DEC 8640 RECEIVER,BUS,QUAD,UNIBUS,Q=BU	6	E48,E62,E25,E31,E37,E41
46	46		1911573-00	74S280 PARITY GEN/CHKR,9BIT ODD/EVEN	4	E42,E49,E56,E63
47	47		1911579-00	8641 TRANSCEIVER,BUS,QUAD,UNIBUS	6	E1,E3,E8,E13,E19,E55
48	48		1911675-00	74S130 DECODER=THREE INPUT	1	E51
49	49		1911944-00	555CN TIMER,FUNCT,BLOCK	1	E5
50	50		1911983-00	74S133 NAND GATE=POSITIVE 13IN	1	E45
51	51	SEE LINE #83.	1912048-02	DEC 7012-02 VOLT.REG.FIX T12V 1.5A T	1	Q2
52	52		1912300-00	74S02 NOR GATE=QUAD 2IN,POS	1	E30
53	53		1912309-00	74S00 AND GATE=QUAD 2IN,POS 14	2	E22,E23
54	54		1912541-00	VOLT.REG.FIX -5V .02A	1	Q1
55	55		1912746-00	DEC 74S37 NAND GATE=QUAD 2IN	1	E12
56	56		1912807-00	LS10 NAND GATE=TRIPLE 3IN	2	E11,E40
57	57		1912828-00	LS05 COMPARATOR,4BIT MAGNITUDE	1	E54
58	58		1912853-00	LS175 FF-D QUAD	2	E10,E15
59	59		1912867-00	LS290 MUX 1 OF 4,2IN W/STORAGE	2	E21,E27
60	60		1913340-00	74S32 OR GATE=QUAD 2IN	2	E35,E36
61	61		1913462-00	74S240 OCTAL BUFFER,INVERTING TRI=STA	1	E52
62	62		1913670-00	74S373 LATCH 8BIT TRASP TRI=STATE	3	E50,E57,E64
63	63		1913777-00	LS240 DRIVER,LINE,OCTAL,TRI=ST	9	E24,E60,E69,E86,E119,E136,
					CONT	E169,E186,E203
64	64		1914086-00	74S30 NAND GATE=POS 8IN	1	E60
65	65		1914451-00	74LS393 COUNTER,BINARY,4BIT	1	E43
66	66		1915193-00	LS244 DRIVER,LINE,OCTAL,TRI=ST	1	E17
67	67		1915219-00	LS373 FF-D OCTAL=TRANSPARENT	8	E2,E4,E9,E14,E20,E26,E32,E38
68	68		23249F1-00	F1-01 PROM, 1	1	E67
69	69		23468A2-00	A2-05 PROM,	1	E66
70	70		7414765-00	HEATSINK	1	
71	71		9000024-01	EYFLET, ROLLED FLANGE, .121 OD X .196 LG	12	
72	72		9010092-00	SCREW,PAN ,PHIL, 4-40X 5/16 SS	1	
73	73		9007201-00	TRANSIPADS #10253	1	
74	74		9009140-00	PJH, STAKING, P.C. BOARD, .025 X .025	5	
75	75		9009105-00	JUMPER, WIRE, INSULATED, BLACK BAND	11	W2,W7,W10-W16,W20,W21

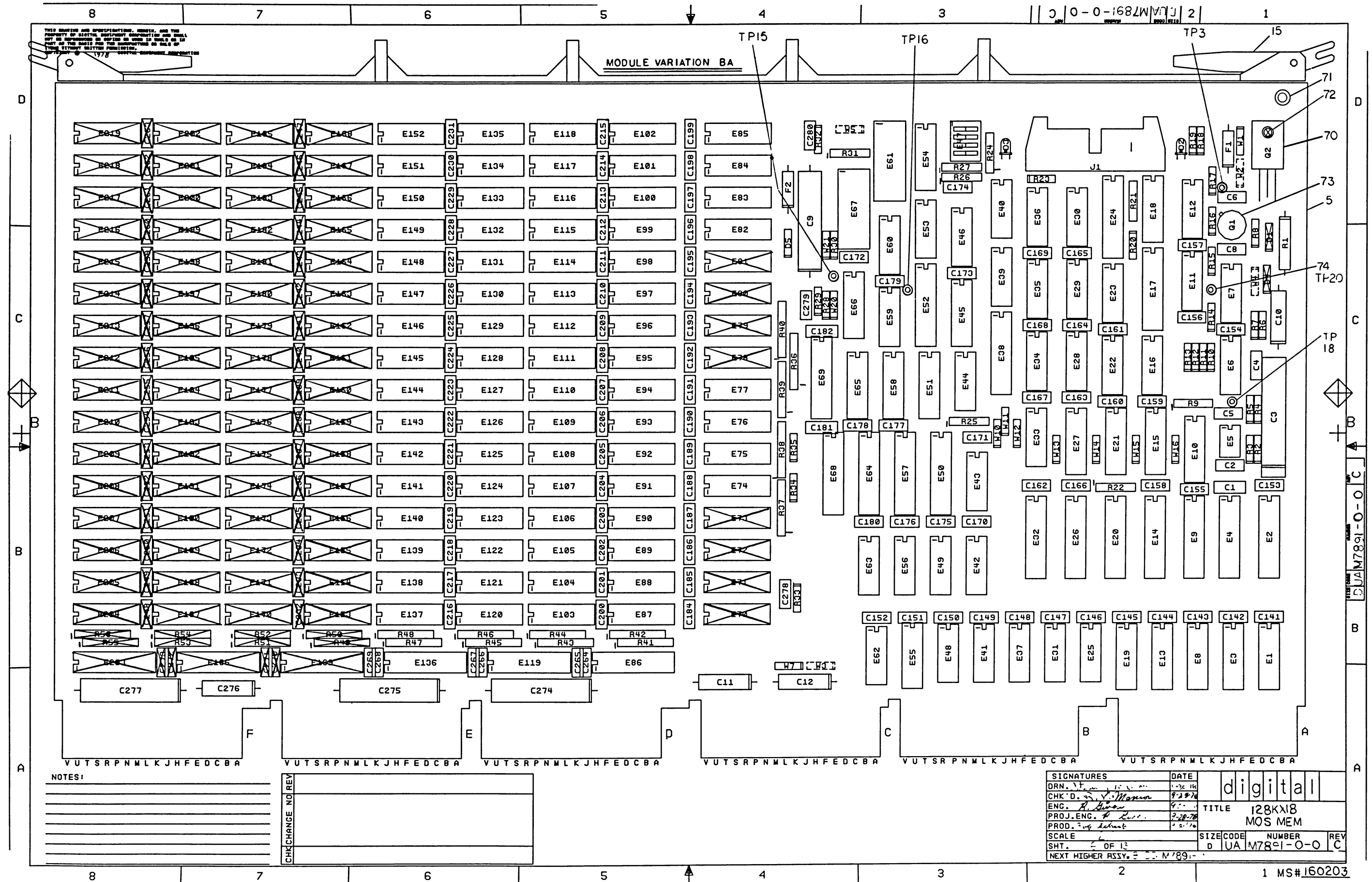
	TITLE	PARTS LIST	SIZE	CODE	DOCUMENT NUMBER	REV
DIGITAL EQUIPMENT CORPORATION		MS11-LD 128K X 10 MOS MEMORY				
MAYNARD, MASSACHUSETTS			K	PL	M7091-DC-DBP	A

LINE	ITEM	DOCUMENT NO.	PART NO.	DESCRIPTION	QTY	REFERENCE DESIGNATORS
76	76		1109991-00	1N 754A VZ= 6.8 5% .40W	1	D5
77	77		1105275-00	***** THIS ITEM IS NOT USED *****	-	
78	78		1210929-04	FUSE, SUB-MINI .250A, 125V, AXIAL LEAD	1	F2
79	79		2114408-01	16K MOS RAM 200NS 16PIN DYNA	144	E70=E85,E120=E135,E170=E185,
					CONT	E87=E118,E137=E168,E187=E202,
					CONT	E204=E219
80	80		1301969-00	22 1/4W 5% CC (13=00	1	R34

81 NOTE: M7891-DA IS A PRIMARY VARIATION OF THE 128K X 18 BIT SYSTEM (NOT A MODULE TYPE).
82 NOTE: M7891-DC IS A MODULE TYPE USING FUJITSU 16K MOS DEVICES.
83 NOTE: 1912048-05 MAY BE SUBSTITUTED FOR ITEM 51 PART #1912048-02.

	TITLE	PARTS LIST	SIZE	CODE	DOCUMENT NUMBER	REV
DIGITAL EQUIPMENT CORPORATION		M611-LD 128K X 18 MOS MEMORY	K	PL	M7091-DC-DDP	A
MAYNARD, MASSACHUSETTS						





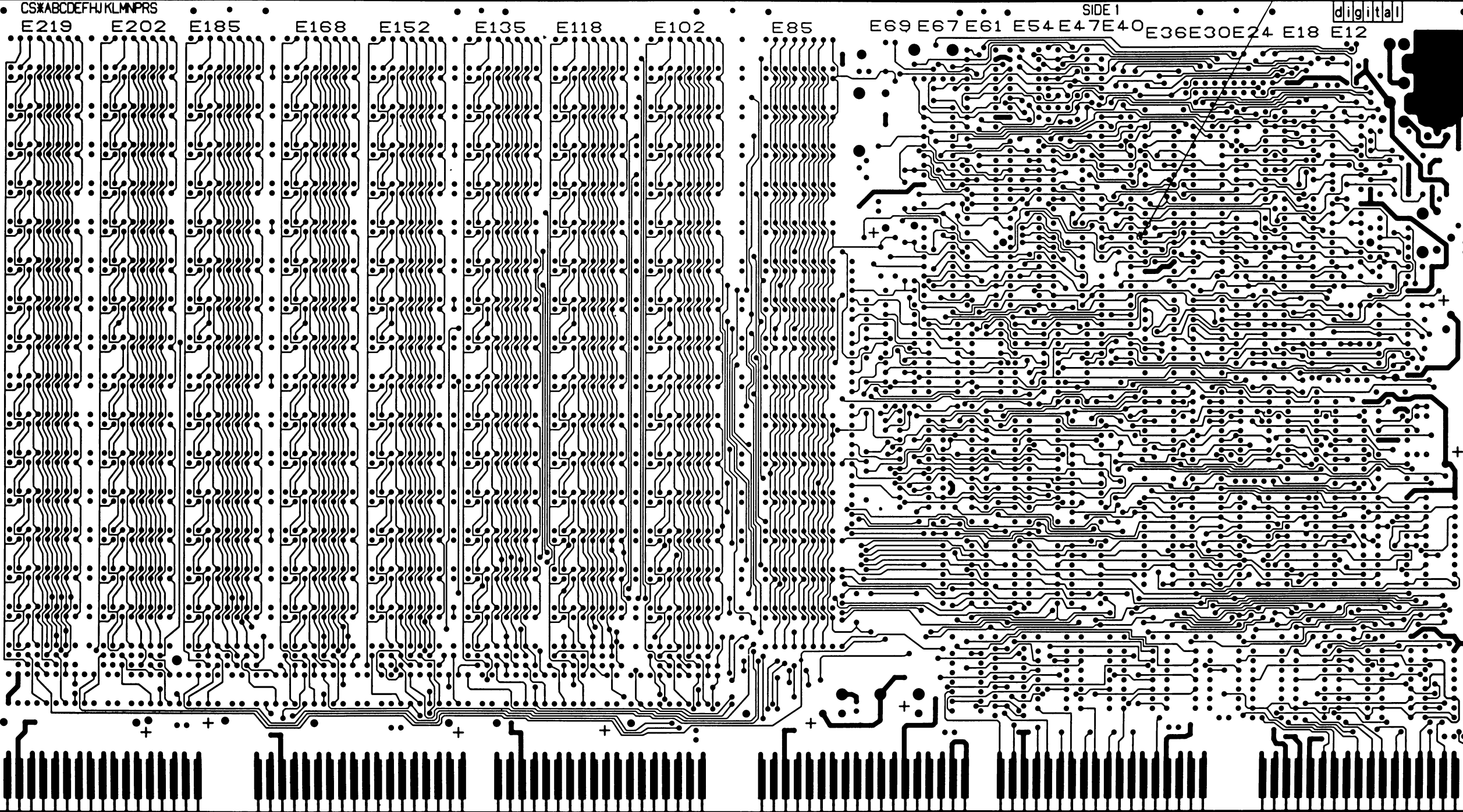
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12 / 13 MIL
M7891 5013399 B

LAYER 1

0-0-1682 M7891-0-0

L1



REVISION			TITLE				SIZE CODE		NUMBER		REV
1	2	3	128K X 18 MOS MEM				DUA		M7891-0-0		C
SCALE			2 / 1		SHEET		9 OF 13		DIST		

[illegible]

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NOTES:

1.

STARTING ADDRESS		SWITCH SETTING (X = OFF)								
DEC (K)	OCTAL	S2-1	S2-2	S2-3	S2-4	S2-5	S2-6	S2-7	S2-8	S2-9
0	00000000									
4	00020000									X
8	00040000								X	
12	00060000								X	X
16	00100000							X		
20	00120000							X		X
24	00140000							X	X	
28	00160000							X	X	X
32	00200000						X			
36	00220000						X			X
40	00240000						X		X	
44	00260000						X		X	X
48	00300000						X	X		
52	00320000						X	X		X
56	00340000						X	X	X	
60	00360000						X	X	X	X
64	00400000					X				
68	00420000					X				X
72	00440000					X			X	
76	00460000					X			X	X
80	00500000					X		X		
84	00520000					X		X		X
88	00540000					X		X	X	
92	00560000					X		X	X	X
96	00600000					X	X			
100	00620000					X	X			X
104	00640000					X	X		X	
108	00660000					X	X		X	X
112	00700000					X	X	X		
116	00720000					X	X	X		X
120	00740000					X	X	X	X	
124	00760000					X	X	X	X	X

STARTING ADDRESS RANGE		SWITCH SETTING (X = OFF)								
DEC (K)	OCTAL	S2-1	S2-2	S2-3	S2-4	S2-5	S2-6	S2-7	S2-8	S2-9
128-252	01000000-01760000				X	TO OBTAIN INCREMENTAL 4K BOUNDARIES WITHIN THE SPECIFIED RANGE, REPEAT SWITCH SETTINGS FROM THE 0-124 K TABLE. I.E. S.A. = 260 K S2-3 = X = OFF S2-9 = X = OFF				
256-380	02000000-02760000			X						
384-508	03000000-03760000			X	X					
512-636	04000000-04760000		X							
640-764	05000000-05760000		X		X					
768-892	06000000-06760000		X	X						
896-1020	07000000-07760000		X	X	X					
1024-1148	10000000-10760000	X								
1152-1276	11000000-11760000	X			X					
1280-1404	12000000-12760000	X		X						
1408-1532	13000000-13760000	X		X	X					
1536-1660	14000000-14760000	X	X							
1664-1788	15000000-15760000	X	X		X					
1792-1916	16000000-16760000	X	X	X						
1920-2044	17000000-17760000	X	X	X	X					

TO OBTAIN INCREMENTAL 4K BOUNDARIES WITHIN THE SPECIFIED RANGE, REPEAT SWITCH SETTINGS FROM THE 0-124 K TABLE.
I.E.
S.A. = 260 K
S2-3 = X = OFF
S2-9 = X = OFF

3. EUB CSR ADDRESS		MOD. UNIBUS CSR ADDRESS		SWITCH SETTING (X = OFF)			
OCTAL		OCTAL		SI-1	SI-2	SI-3	SI-4
17772100	772100						
17772102	772102						X
17772104	772104					X	
17772106	772106					X	X
17772110	772110			X			
17772112	772112			X			X
17772114	772114			X	X		
17772116	772116			X	X	X	X
17772120	772120			X			
17772122	772122			X			X
17772124	772124			X		X	
17772126	772126			X		X	X
17772130	772130			X	X		
17772132	772132			X	X		X
17772134	772134			X	X	X	
17772136	772136			X	X	X	X

OPTION DESIGNATION	PRIMARY VARIATION	SYSTEM DESCRIPTION
MS11-LA	M7891-AA	32K X 18 BITS
MS11-LB	M7891-BA	64K X 18 BITS
MS11-LC	M7891-CA	96K X 18 BITS
MS11-LD	M7891-DA	128K X 18 BITS

5. BUS VOLTAGE		JUMPER	
		W1	W2
+ 12V		IN	OUT
+ 15V		OUT	IN

6. BUS VOLTAGE		JUMPER	
		W3	W7
+ 5V		IN	OUT
+ 5BBU		OUT	IN

7. PERIPHERAL PAGE SIZE		JUMPER	
		W5	W21
2K		IN	IN
4K		OUT	IN
8K		OUT	OUT

8. FUNCTION		JUMPER		
		W10	W11	W12
NORMAL		IN	IN	IN
ROW ADDR DISABLE		IN	IN	OUT
COL ADDR DISABLE		IN	OUT	IN
REF ADDR DISABLE		OUT	IN	IN

9. FUNCTION		JUMPER			
		W13	W14	W15	W16
NORMAL		IN	IN	IN	IN
LAT DATA DISABLE		OUT	IN	IN	IN
CSR DATA DISABLE		IN	OUT	IN	IN
CSR DATA DISABLE		IN	IN	OUT	IN
X-ADDR DISABLE		IN	IN	IN	OUT

10. TYPE		JUMPER	
		W4	
MOD UNIBUS		OUT	
EUB		IN	

11. FUNCTION		JUMPER	
		W20	
NORMAL		IN	
SSYN DISABLE		OUT	

12. IC TYPE	+ 5V	GND	+12V	-5V
MOS	9	16	8	1
74S00	14	7		
74S10	14	7		
74S11	14	7		
74S20	14	7		
74S03	14	7		
74S74	14	7		
74S74-01	14	7		
74S158	16	8		
74LS175	16	8		
8640	8	1		
8641	16	8		
74S280	14	7		
74138	16	8		
555	1		8	
74S02	14	7		
74S08	14	7		
74S37	14	7		
74LS10	14	7		
74LS85	16	8		
74LS298	16	8		
74S32	14	7		
74S240	20	10		
74LS240	20	10		
74S373	20	10		
74S30	14	7		
74LS393	14	7		
74LS244	20	10		
74LS373	20	10		
74S133	16	8		
1K X 4 PROM	18	9		
256 X 4 PROM	16	8		

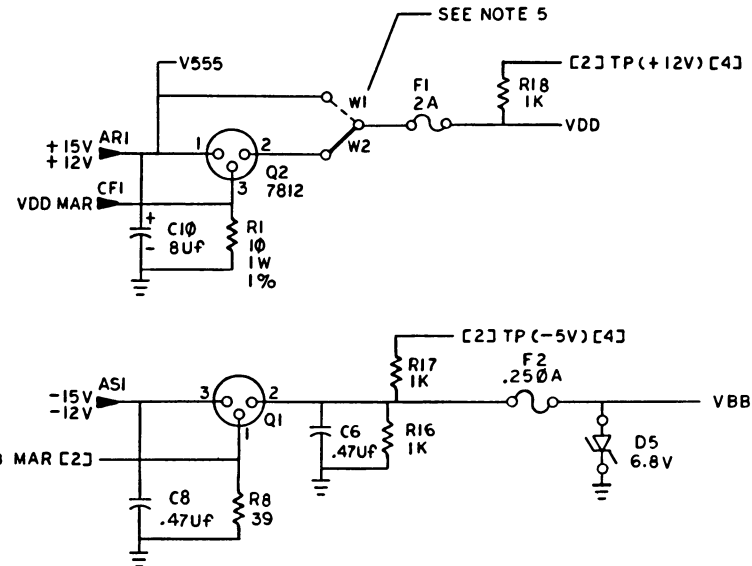
13. SIGNAL NAMES WILL BE REFERENCED AS FOLLOWS:
[X] SIGNAL NAME [Y/Z]
NUMBER OF CONNECTION POINTS ON DESTINATION SHEET.
DESTINATION SHEET NUMBER.
SOURCE SHEET NUMBER.

14. * INDICATES BATTERY BACK UP (+5V CR)
● INDICATES .125 PAD ON SIDES 1 AND 2.
⊙ INDICATES WIRE WRAP PINS AND TEST POINTS.
15. RESISTORS ARE 5% UNLESS OTHERWISE SPECIFIED.

A		REV.	
CHK	CHANGE NO.	REV.	DATE
602	M7891-M1001	B	9/24/78
602	M7891-M1002	C	9/28/78
602	M7891-M1003	D	10/11/78

DRN By: J. Egan	6-30-78	FIRST USED ON	11/34	digital
CHK'D By: J. Egan	9/24/78	TITLE	28K X 18 BIT MOS MEM	
ENG By: J. Egan	9-28-78	PROJ ENG By: J. Egan	9-28-78	
PROD By: J. Egan	9-28-78	NEXT HIGHER ASSY.		
B-DD-M7891-0		SIZE CODE	NUMBER	REV.
SCALE		D	CS M7891-0-1	C
SHEET 1 OF 14		DIST		

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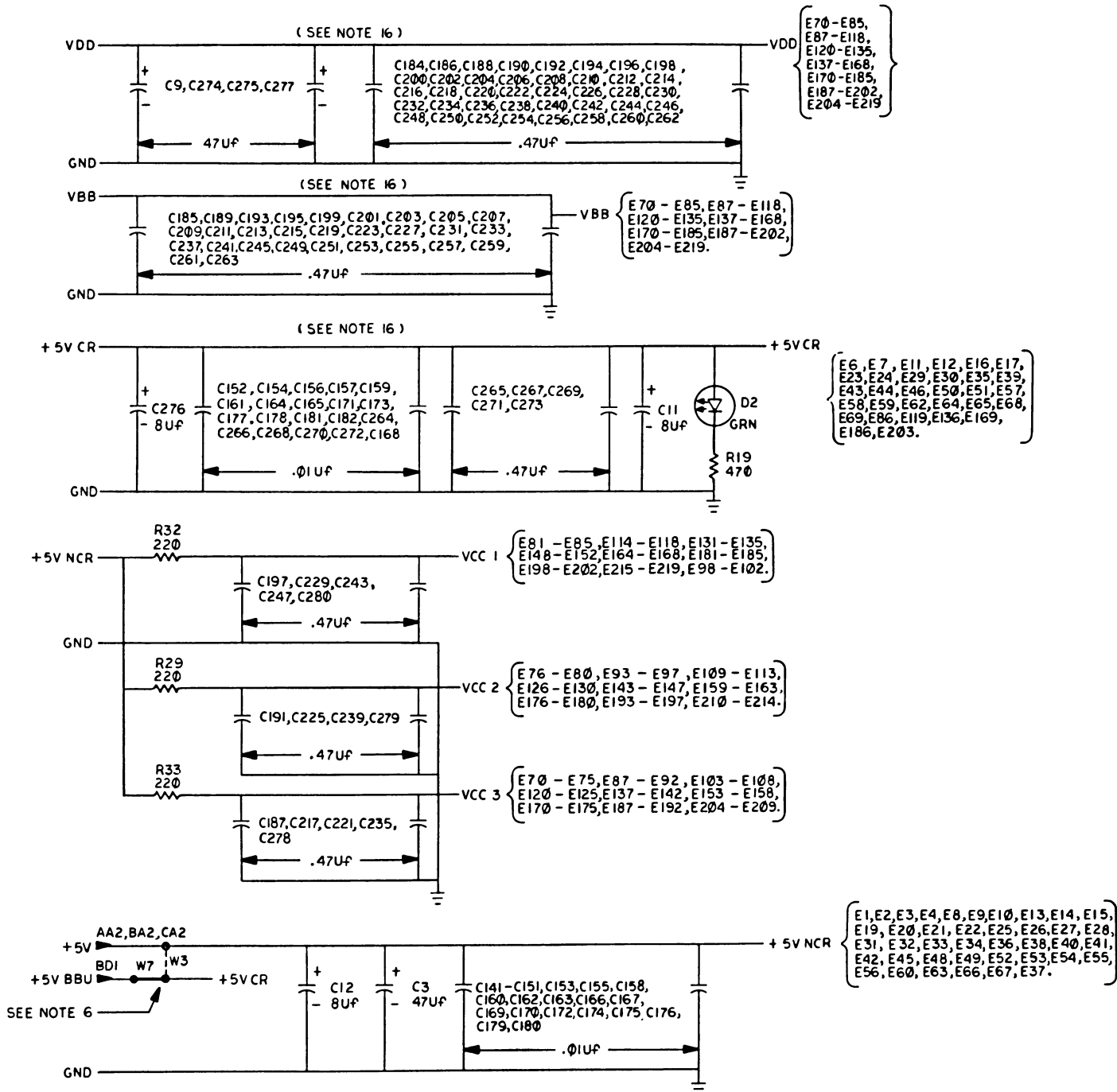


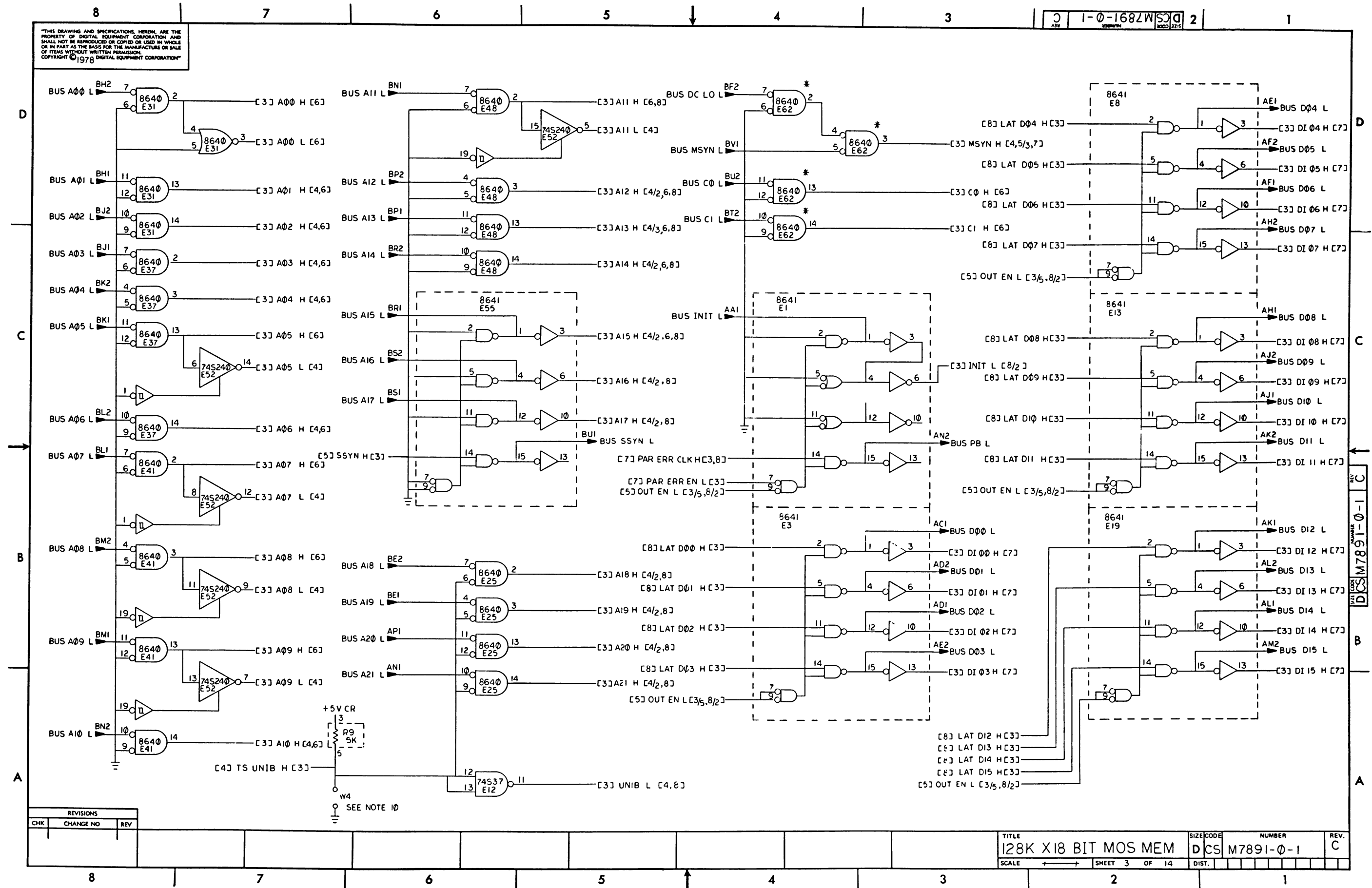
AC2,AT1,BC2,BT1,
CC2,CT1,DC2,DT1,
EC2,ET1,FC2,FT1

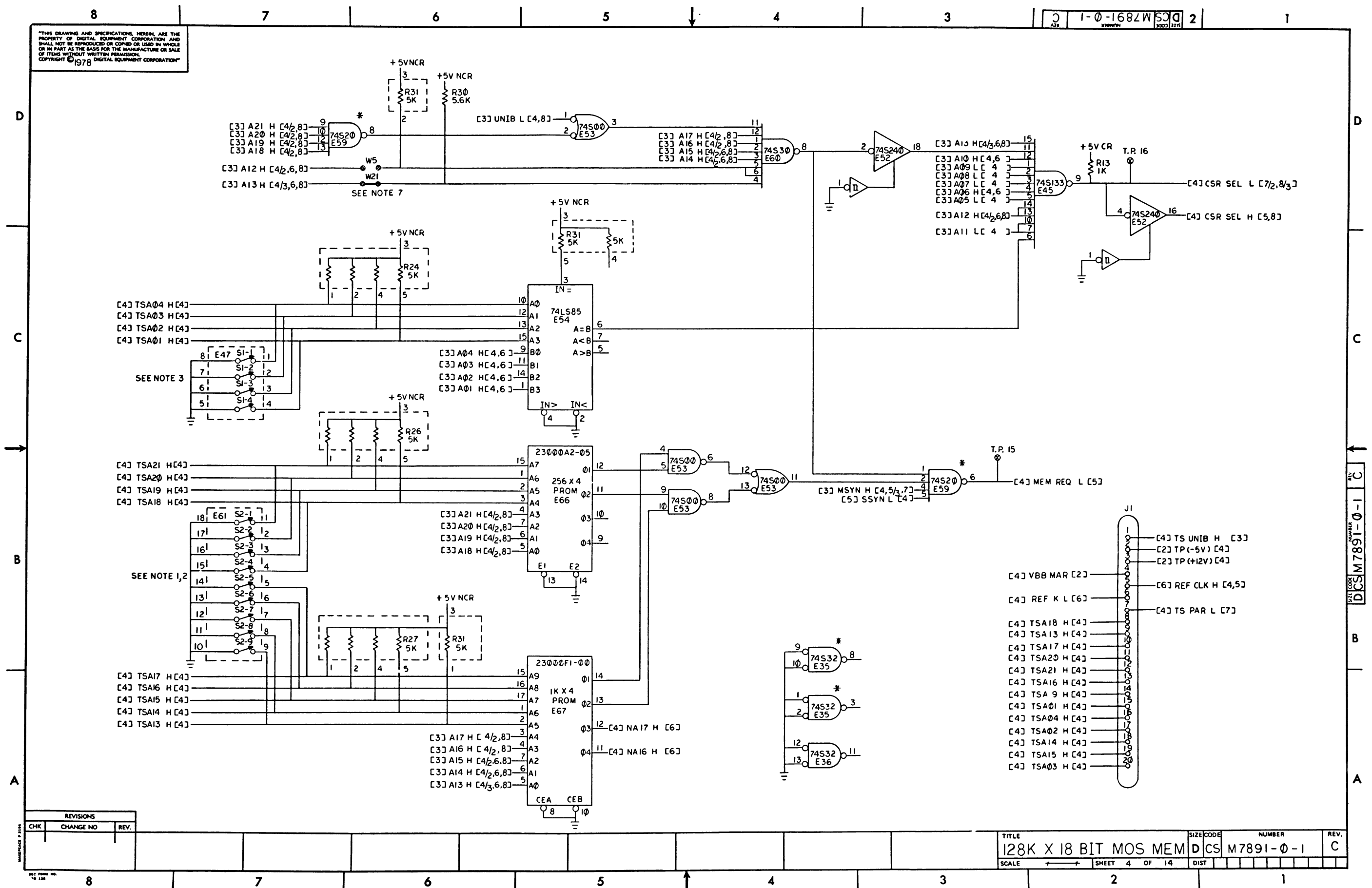
GND

BUS GRANT LINES

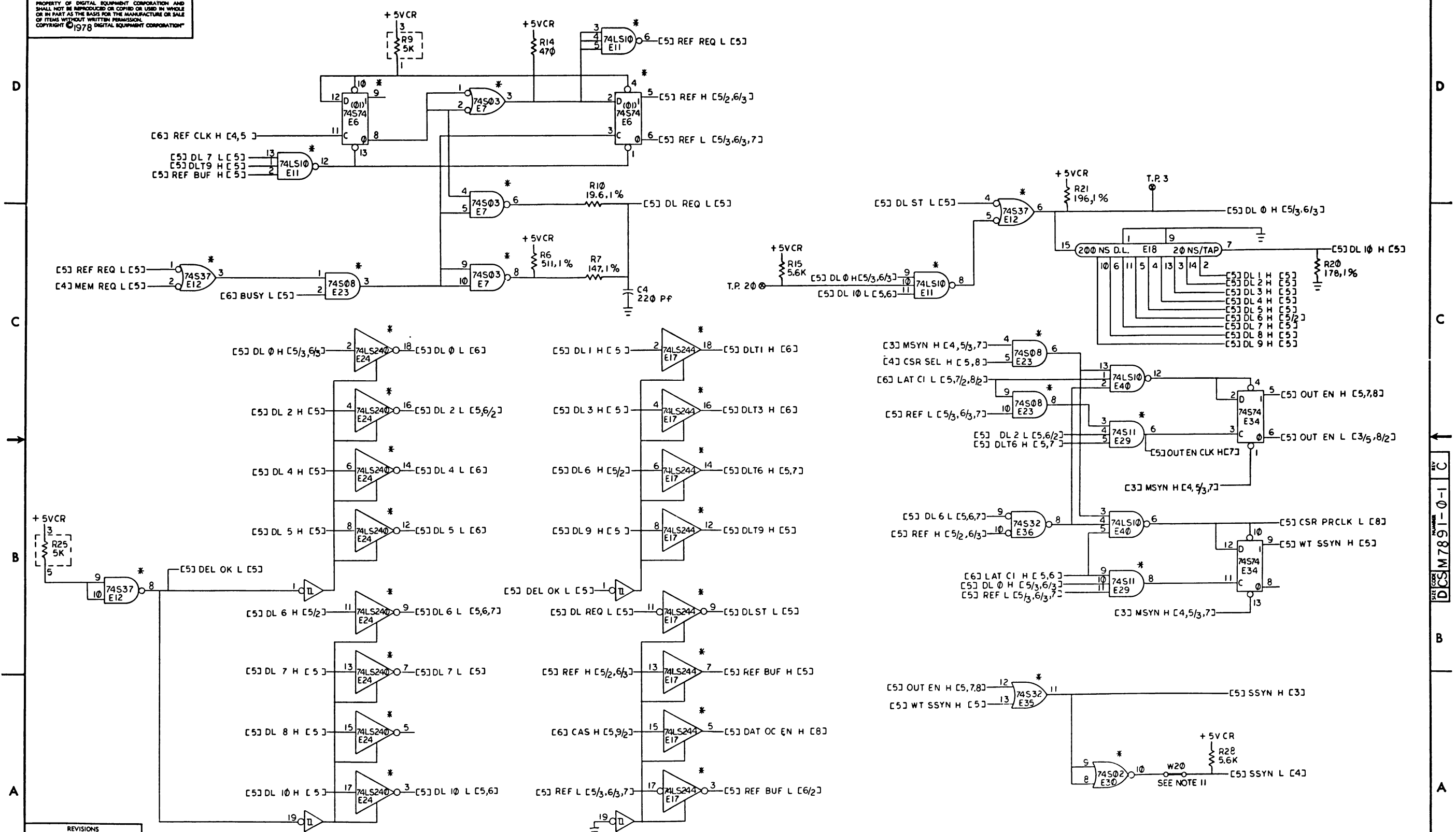
DK2 DL2
DP2 DR2
DM2 DN2
DS2 DT2
CA1 CB1





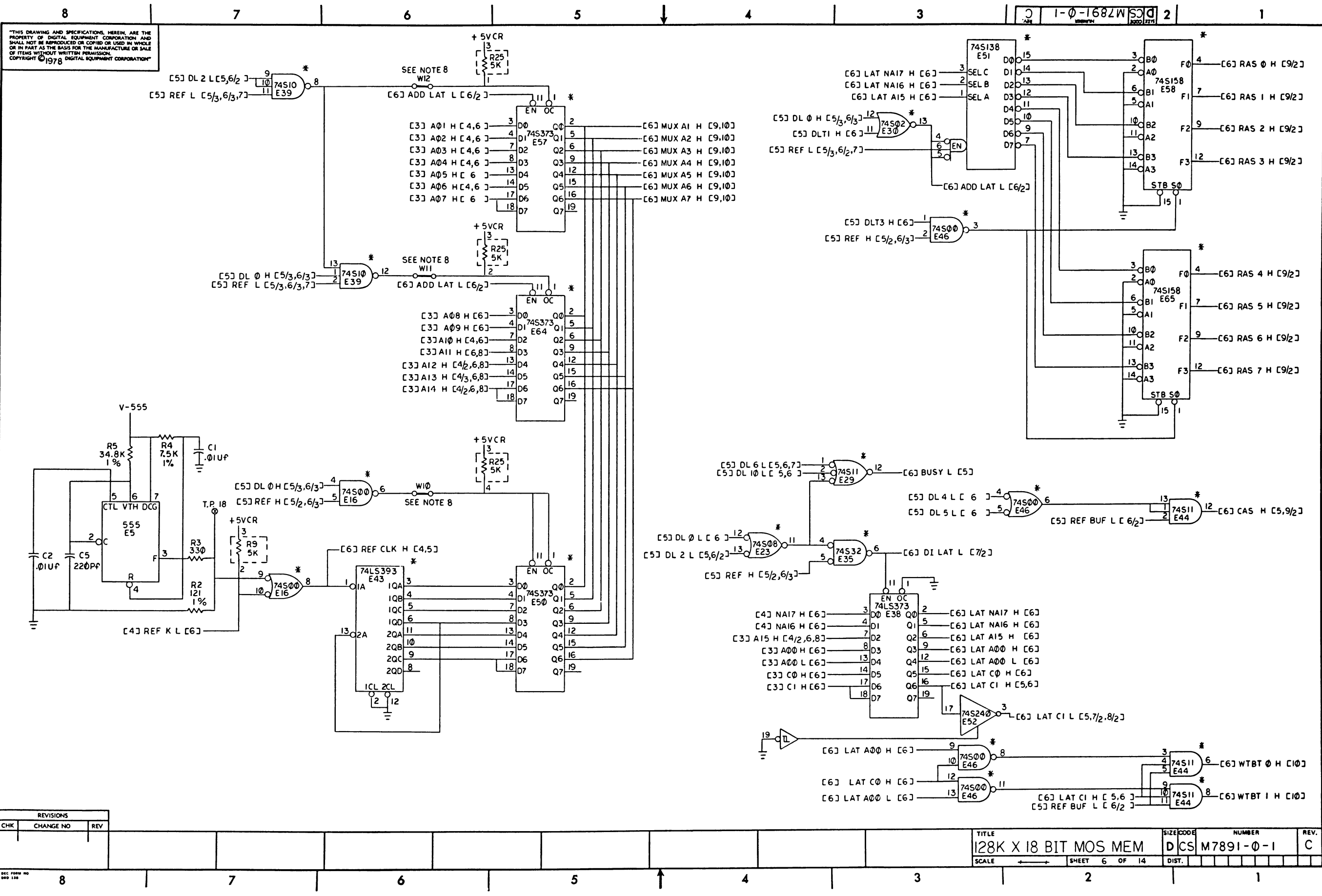


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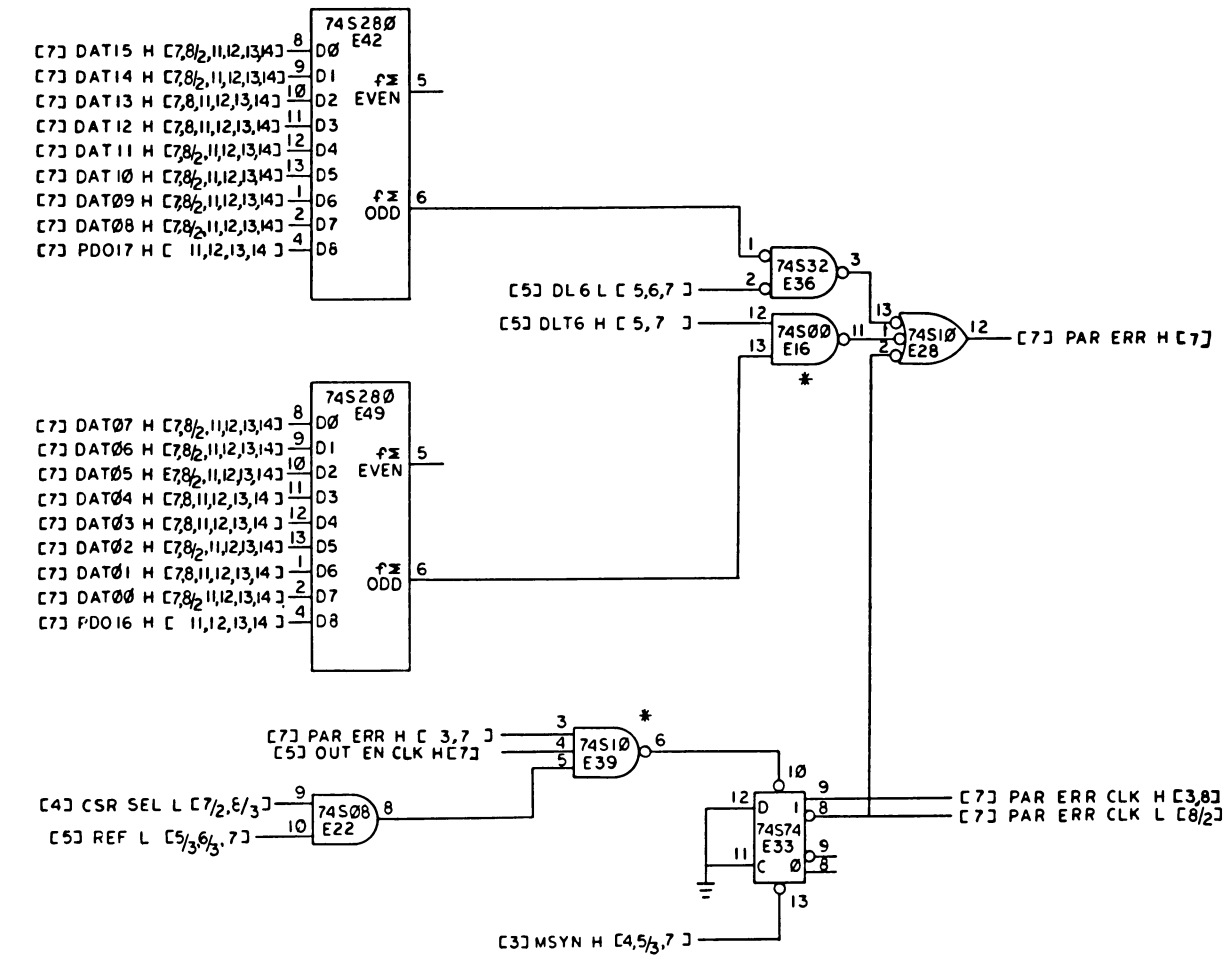
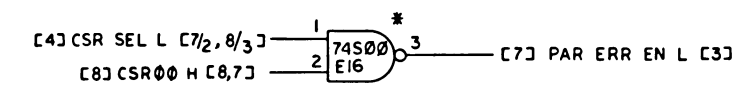
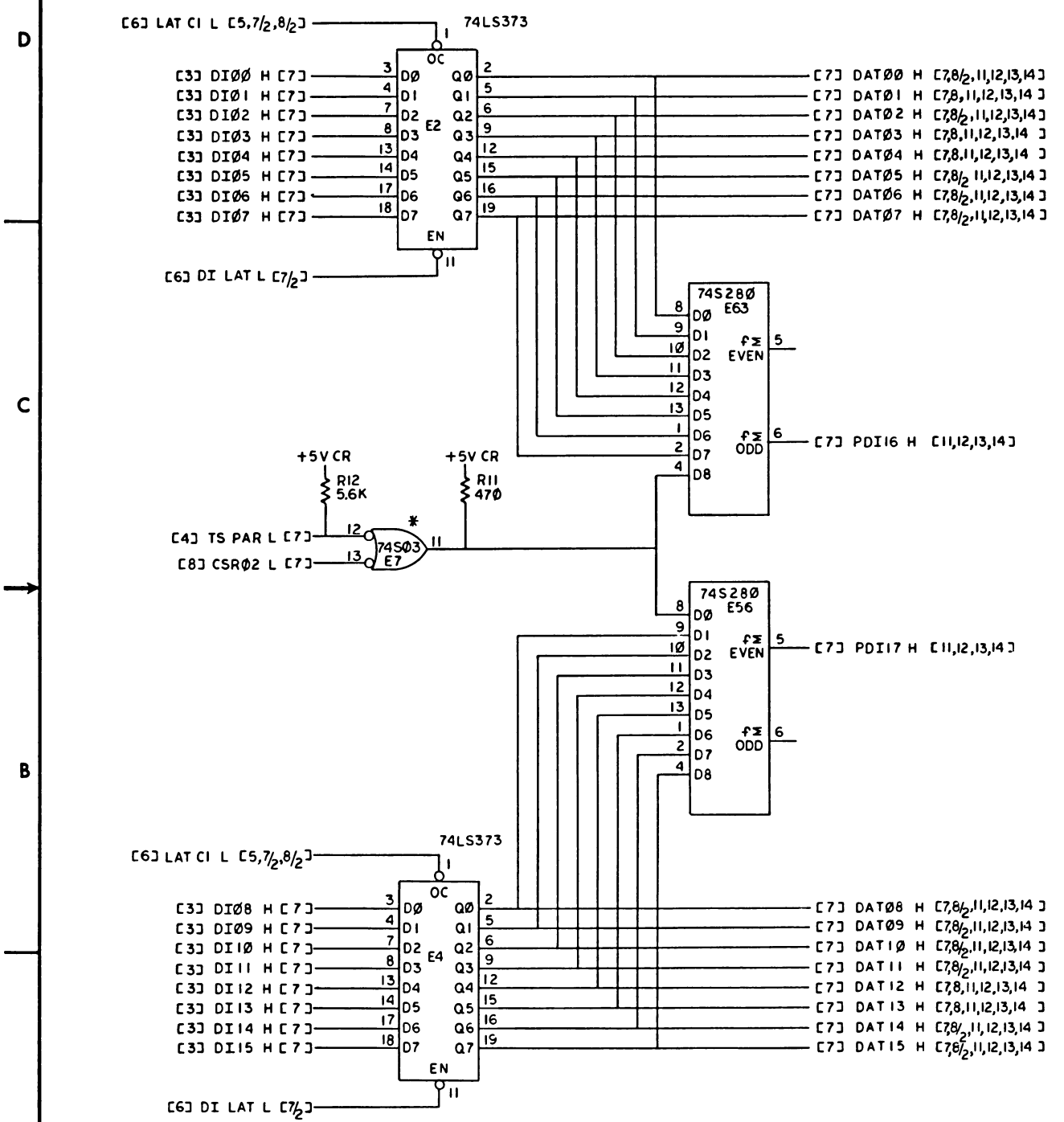
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SCALE	SHEET	5 OF 14	DIST.	



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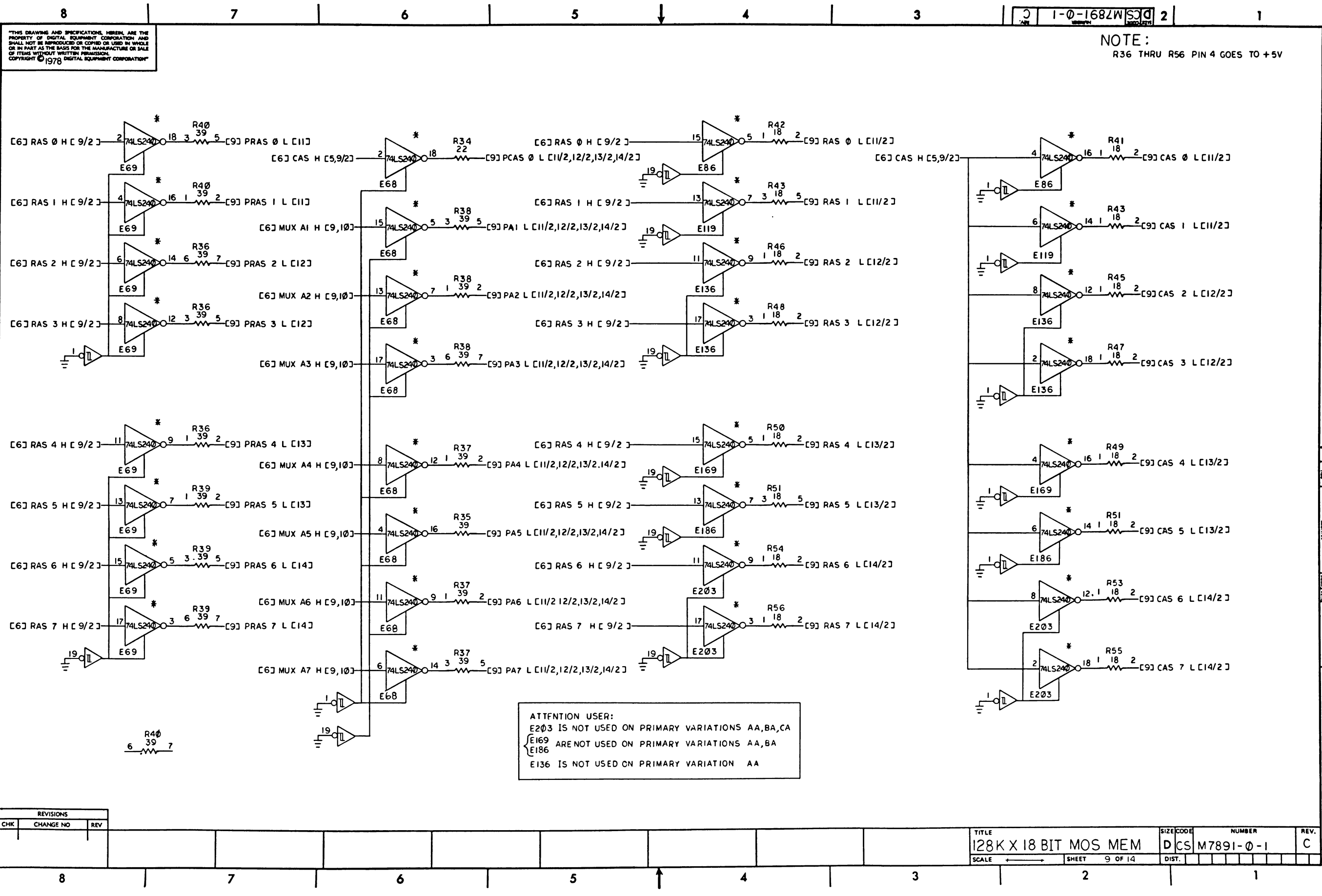
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REVISIONS		
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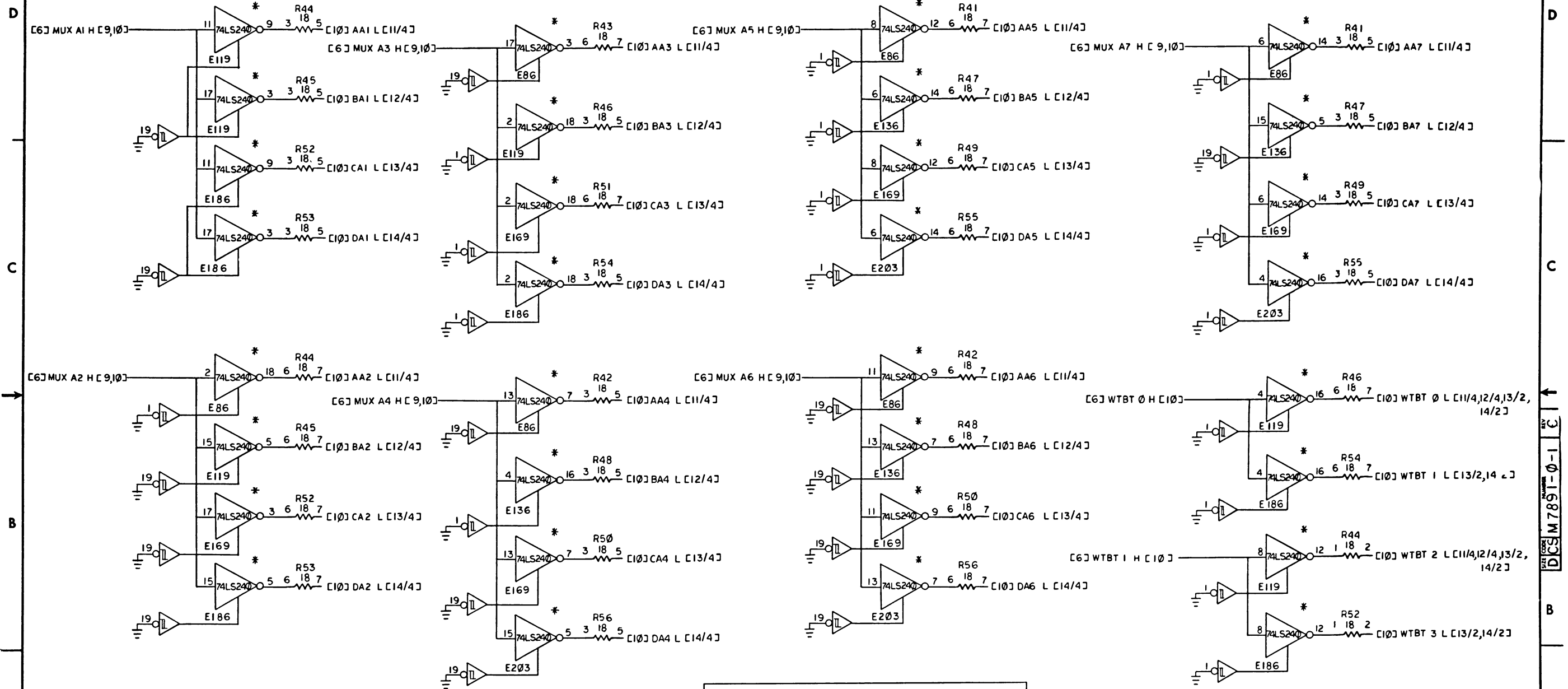
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SCALE ————	SHEET 7 OF 14	DIST.		



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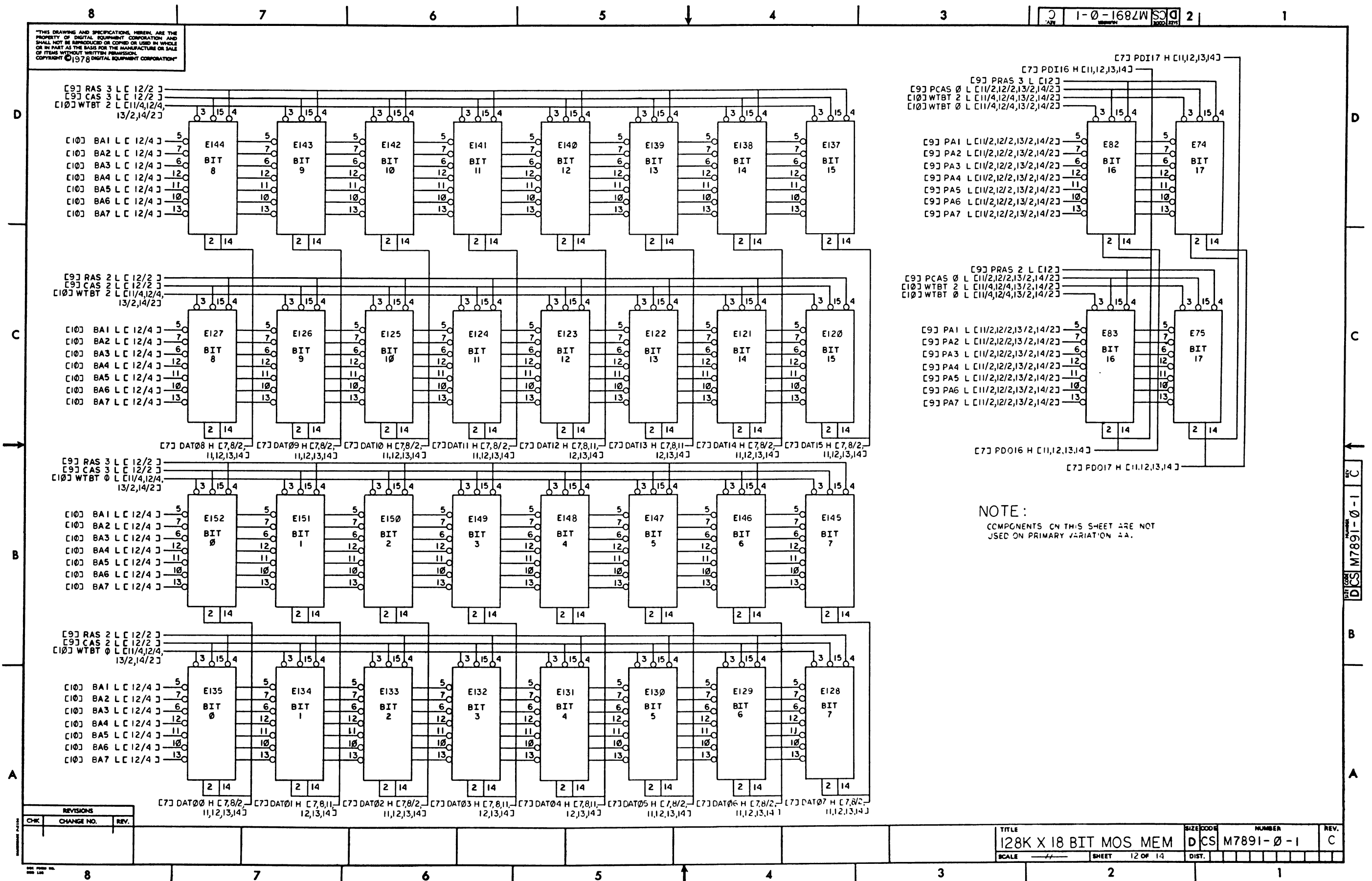
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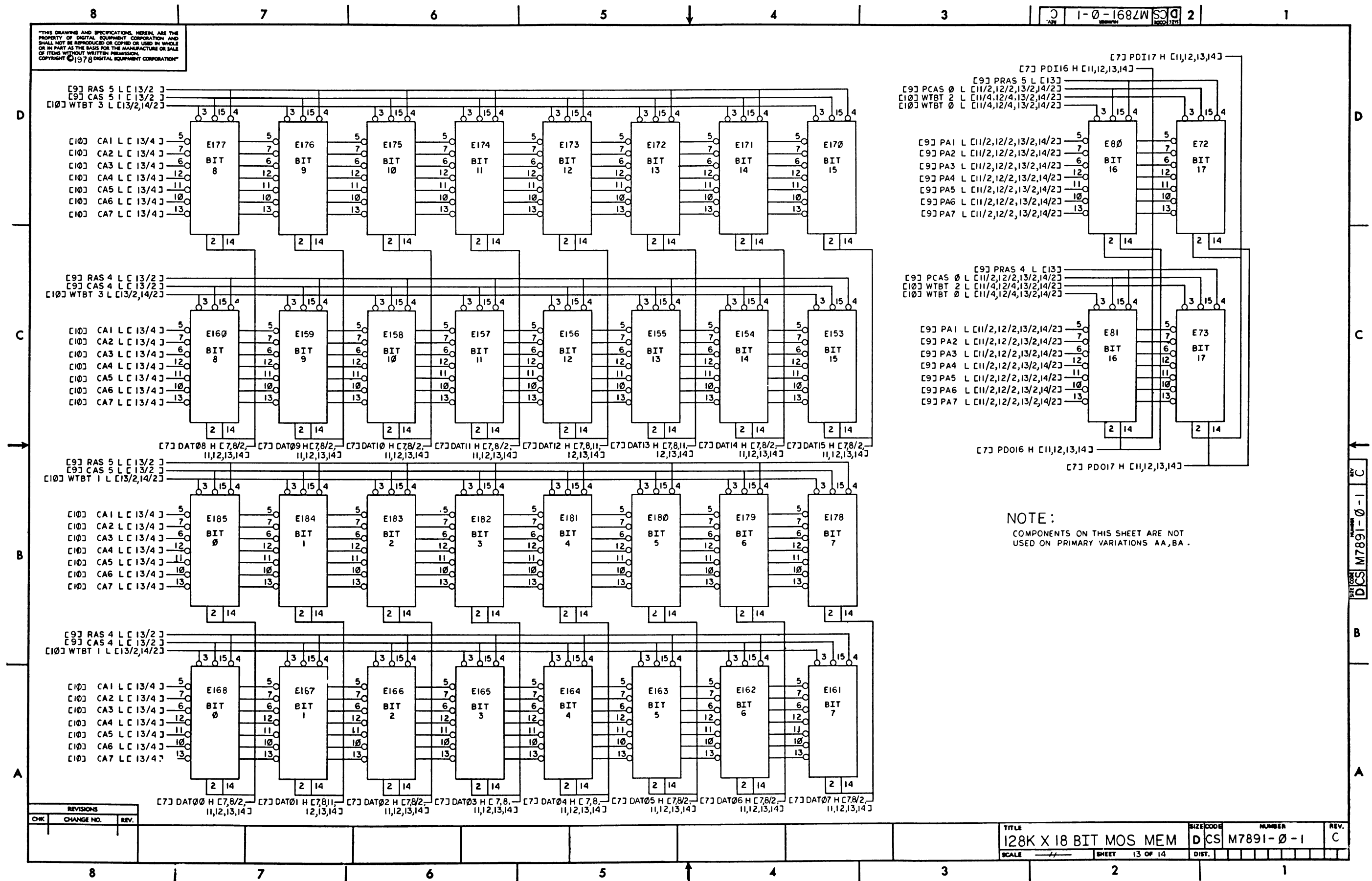
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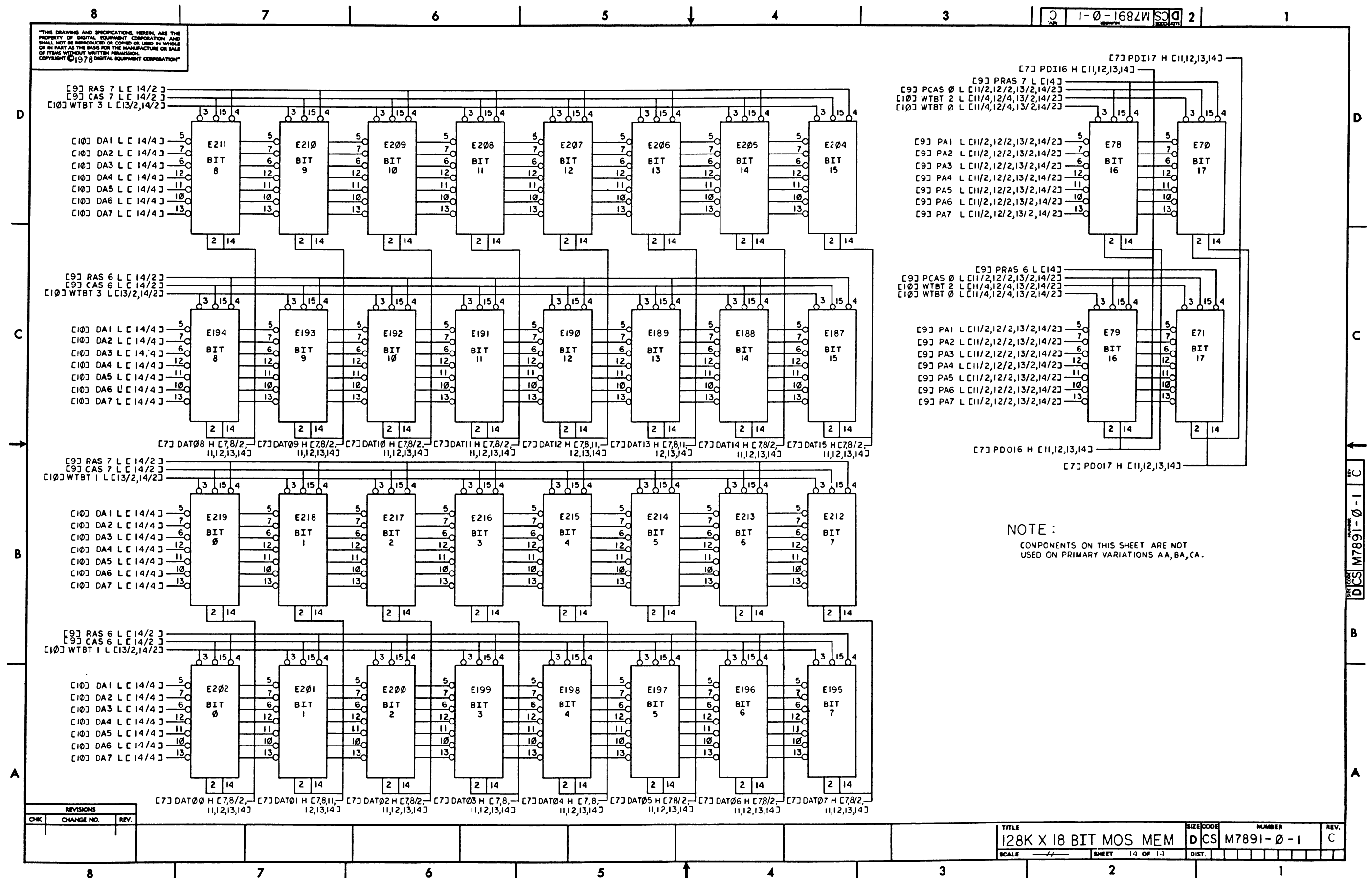


ATTENTION USER:
E203 IS NOT USED ON PRIMARY VARIATIONS AA,BA,CA
E169 ARE NOT USED ON PRIMARY VARIATIONS AA,BA
E186 IS NOT USED ON PRIMARY VARIATION AA

REVISIONS				TITLE				SIZE CODE				NUMBER				REV.			
CHK	CHANGE NO	REV		128K X 18 BIT MOS MEM				DCS				M7891-0-1				C			
				SCALE				SHEET 10 OF 14				DIST.							







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